**IN THE CLAIMS**

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1. (Currently Amended) A computer system comprising:

a decode unit for decoding instructions fetched from a memory holding a sequence of instructions, all instructions in the sequence having the same predetermined bit length; and

first and second processing channels, each channel comprising a plurality of functional units, at least one of said functional units in each channel being a data processing unit and at least one other of said functional units in each channel being a memory access unit;

wherein the decode unit is operable to detect for each instruction of said predetermined bit length whether the instruction defines a single operation or two independent operations and to control the first and second channels in dependence on said detection~~.~~;

said decode unit being operable to control the first and second channels such that, when the decode unit detects that the instruction defines two independent operations, it is operable to control the first channel to implement one of those operations and the second channel to implement the other of those operations, whereby the first and second channels execute their respective independent operations simultaneously; and

said decode unit being further operable to control the first and second channels such that, when the decode unit detects that the instruction defines a single operation, it controls the first and second channels each to cooperate to simultaneously execute said single operation.

2. (Canceled)

3. (Canceled)

4. (Original) A computer system according to claim 1, wherein the first and second channels share at least one common register file and can simultaneously access said register file.

5. (Original) A computer system according to claim 1, wherein the decode unit is operable to make said detection based on the values of a designated set of identification bits at predetermined bit locations in the instruction.

6. (Original) A computer system according to claim 5, wherein, when the instruction has a length of n bits, the predetermined bit locations include the n/2th bit and the nth bit.

7. (Original) A computer system according to claim 1, wherein the decode unit is operable to identify certain combinations of said independent operations in an instruction based on said set of identification bits, wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation and a fourth combination denotes a long instruction.

8. (Original) A method of operating a computer system which comprises first and second processing channels each having a plurality of functional units including at least one data processing unit and one memory access unit, the method comprising:

decoding an instruction having a predetermined bit length to detect whether that instruction defines a single operation or two independent operations;

where the instruction defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously; and

when the instruction defines a single operation, controlling the first and second processing channels to cooperate to implement said single operation.

9. (Original) A method according to claim 8, wherein the step of decoding and detecting comprises reading the values of a designated set of bits at predetermined bit locations in the instruction.

10. (Original) A method according to claim 9, wherein said designated bits are used to denote the nature of independent operations when the instruction defines two operations, in addition to designating that the instruction defines a single operation.

11. (Original) A method according to claim 8, wherein, for an instruction having n bits, the predetermined bit locations include the n/2th bit and the nth bit.

12. (Currently Amended) A computer program product comprising

program code means which include a sequence of instructions all having the same predetermined bit length, said instructions including long instructions wherein said predetermined bit length defines a single operation and dual operation instructions, wherein said predetermined bit length defines two independent operations,

wherein the computer program product is adapted to run on a computer such that a long instruction defining a single operation controls ~~the resources of the computer in a first way and~~ a first and second processing channel to cooperate to implement said single operation, the first and second processing channels each having a plurality of functional units including at least one data processing unit and one memory access unit;

and wherein the computer program product is further adapted to run on a computer such that a dual operation instruction defining two independent operations controls the ~~resources of the computer in a second way, and~~ first and second processing channels such that one of the operations is supplied to the first processing channel and the other of the operations is supplied to the second processing channel, whereby the operations are executed simultaneously; and

wherein each instruction of said predetermined bit length includes a set of identification bits at designated bit locations within the instruction, said identification bits being adapted to cooperate with a decode unit of a computer system to designate whether the instruction is a long instruction or a dual operation instruction.

13. (Canceled)

14. (Currently Amended) A computer program product according to claim 12 ~~13~~, wherein said designated bit locations in an instruction of n bits include at least n/2th and nth bit.

15. (Currently Amended) A method of operating a computer system which comprises first and second processing channels each having a plurality of functional units including at least one data processing unit and one memory access unit, the method comprising:

fetching a sequence of instructions from a program memory, all said instructions having the same predetermined bit length and containing a set of designated bits at predetermined bit locations within said bit length;

decoding each instruction, said decoding step including reading the values of said designated bits to determine:

a) whether the instruction of said predetermined bit length defines a single operation or two independent operations; and

b) where the instruction of said predetermined bit length defines two independent operations, the nature of each of those operations selected at least from a data processing category of operation and a memory access category of operation~~.~~; and

when the instruction of said predetermined bit length defines two independent operations, supplying one of the operations to the first processing channel and the other of the operations to the second processing channel whereby the operations are executed simultaneously; and

when the instruction of said predetermined bit length defines a single operation, controlling the first and second processing channels to cooperate to implement said single operation.

16. (Currently Amended) A computer program product

~~comprising program code means which include a sequence of the instructions all having the same predetermined bit length, said instructions including long instructions wherein said predetermined bit length defines two independent operations, said instructions including a set of identification bits at designated bit locations within the instruction, wherein the computer program product is adapted to run on a computer such that said identification bits are adapted to cooperate with a decode unit of the computer to designate whether:~~

~~a) the instruction is a long instruction or a dual operation instruction; and~~

~~)~~

according to claim 12, wherein said designated bit locations identify, in the case of a dual operation instruction, the nature of each operation in the instruction, said nature being selected from a data processing category and a memory access category.